

## WHAT IS CLAIMED IS :

1. A cross-bar switch system with redundancy having a cross-bar switch set of a redundant structure comprising a plurality of cross-bar switches necessary for effecting connections between nodes of a plurality of nodes, and at least one additional 5 redundant cross-bar switch;

(a) wherein a first cross-bar switch of said cross-bar switch set receives at input terminals thereof, first outputs among multiple  $N$  outputs of each of the plurality of nodes, and said one redundant cross-bar switch receives  $N$ th outputs among 10  $N$  outputs of each of said plurality of nodes applied to input terminals thereof,  $N$  being an integer of 2 or more;

(b) each of the remaining cross-bar switches has  $M$  selection circuits to each of which receives two consecutive outputs of an order corresponding to that of the cross-bar 15 switch, among  $N$  outputs of each of said plurality of nodes, the outputs of these  $M$  selection circuits being input to the cross-bar switch provided that  $M$  is an integer of 2 or more;

(c) each node of said plurality of nodes has  $N$  selection switches, which are provided at input terminals thereof, each 20 of said selection switches receives two consecutive outputs of an output order corresponding to that of the node, among outputs of two mutually adjacent cross-bar switches, two by two, of said cross-bar switch set; and

(d) in response to a selection control signal output from

25 a failure processing circuit that executes cross-bar switch failure processing, each of said selection circuits selects and outputs one of its two inputs and, when one cross-bar switch fails, takes the failed cross-bar switch out of service.

2. A cross-bar switch system with redundancy,

- (a) comprising  $N+1$  cross-bar switches wherein one cross-bar switch is redundantly provided in addition to  $N$  cross-bar switches required for connecting of nodes among first 5 to  $M$ th nodes where  $M$  and  $N$  are prescribed integers equal to or greater than 2, respectively;
- (b) wherein the first cross-bar switch receives each first output among  $N$  outputs of each of said first to  $M$ th nodes at  $M$  input terminals thereof;
- 10 (c) the  $(N+1)$ th cross-bar switch receives each  $N$ th output among  $N$  outputs of each of said first to  $N$ th nodes at  $M$  input terminals thereof;
- (d) an  $I$ th, where  $I$  is an integer of 2 or more and less than  $N$ , cross-bar switch having  $M$  selection circuits, which are 15 provided at respective ones of  $M$  input terminals thereof, to each of which are input consecutive  $(I-1)$ th and  $I$ th outputs, which correspond to said  $I$ th cross-bar switch, among outputs of each of said first to  $M$ th nodes; and
- (e) a  $J$ th, where  $J$  is an integer of 1 or more and not more 20 than  $M$ , node having  $N$  selection switches, which are provided at input terminals of said node, to each of which are input  $J$ th

outputs of two mutually adjacent cross-bar switches among said first to  $(N+1)$  th cross-bar switches, where  $N$  is an integer of 2 or more; and

25 (f) wherein in response to a selection control signal output from a failure processing circuit that executes cross-bar switch failure processing, each of said selection circuits selects and outputs one of its two inputs and, when one cross-bar switch fails, takes the failed cross-bar switch out of service.

3. A cross-bar switch system with redundancy,

(a) comprising  $N+1$  cross-bar switches wherein one cross-bar switch is redundantly provided in addition to  $N$  cross-bar switches required for connecting of nodes among first 5 to  $M$  th nodes, where  $M$  and  $N$  are prescribed integers of 2 or more, respectively;

(b) each node of said first to  $M$  th nodes outputting first to  $M$  th output signals from output terminals thereof and receiving first to  $N$  th input signals applied to input terminals 10 thereof;

(c) the first cross-bar switch receiving each first output signal of each of said first to  $M$  th nodes at  $M$  input terminals thereof;

(d) the  $(N+1)$  th cross-bar switch receiving each  $N$  th 15 output signal of each of said first to  $M$  th nodes at  $M$  input terminals thereof;

(e) an  $l$  th, where  $l$  is an integer of 2 or more and not more

than N cross-bar switch having M selection circuits, which are provided at respective ones of M input terminals thereof, to each 20 of which are input two signals, namely an (l-1)th output signal and an lth output signal, of each of said first to Mth nodes; and

(f) a Jth, where J is an integer of 1 or more and not more than M, node having N selection circuits, which are provided at 25 N input terminals thereof, to each of which are input outputs of a Jth output port of each of mutually adjacent cross-bar switches among said first to (N+1)th cross-bar switches, namely of Kth and (K+1)th cross-bar switches, where K is an integer of 1 or more and not more than N;

30 (g) wherein in response to a selection control signal output from a failure processing circuit that executes cross-bar switch failure processing, each of said selection circuits selects and outputs one of two signals and, when one cross-bar switch fails, takes the failed cross-bar switch out of service.

4. In a system having cross-bar switches for connecting CPUs and a memory within a computer system or for connecting nodes in a computer system composed of a plurality of nodes, a cross-bar switch system with redundancy comprising:

5 (a) N+1 cross-bar switches inclusive of N cross-bar switches that are indispensable for the system and one redundant cross-bar switch;

(b) selection circuits provided at inputs and outputs of

said cross-bar switches; and

10 (c) means, operable when the system fails, for performing control in such a manner that a cross-bar switch that has failed is taken out of service and the redundant cross-bar switch is placed in service by controlling said selection circuits by a failure processing circuit after the system is restarted, said 15 failure processing circuit recognizing that said cross-bar switch has failed.

5. The system according to claim 3, wherein each of said nodes inputs and outputs N bytes of data on a byte-by-byte basis.

6. The system according to any one of claim 1, wherein said failure-processing circuit includes:

an (N+1)-bit cross-bar switch failure information register for storing whether failure has occurred or not with regard to

5 said first to (N+1)th cross-bar switches;

a selection-circuit control output circuit for outputting a selection control signal to each of said selection circuits based upon values in said cross-bar switch failure information register; and

10 a multiple-failure detector for informing a system controller of occurrence of multiple failure when multiple cross-bar switches fail.

7. The system according to claim 2, wherein said failure-processing circuit includes:

an (N+1)-bit cross-bar switch failure information register

for storing whether failure has occurred or not with regard to  
5 said first to (N+1)th cross-bar switches;

a selection-circuit control output circuit for outputting  
a selection control signal to each of said selection circuits  
based upon values in said cross-bar switch failure information  
register; and

10 a multiple-failure detector for informing a system  
controller of occurrence of multiple failure when multiple  
cross-bar switches fail.

8. The system according to claim 3, wherein said failure-  
processing circuit includes:

an (N+1)-bit cross-bar switch failure information register  
for storing whether failure has occurred or not with regard to  
5 said first to (N+1)th cross-bar switches;

a selection-circuit control output circuit for outputting  
a selection control signal to each of said selection circuits  
based upon values in said cross-bar switch failure information  
register; and

10 a multiple-failure detector for informing a system  
controller of occurrence of multiple failure when multiple  
cross-bar switches fail.

9. The system according to claim 4, wherein said failure-  
processing circuit includes:

an (N+1)-bit cross-bar switch failure information register  
for storing whether failure has occurred or not with regard to

5 said first to (N+1)th cross-bar switches;

a selection-circuit control output circuit for outputting a selection control signal to each of said selection circuits based upon values in said cross-bar switch failure information register; and

10 a multiple-failure detector for informing a system controller of occurrence of multiple failure when multiple cross-bar switches fail.

10. The system according to claim 1, wherein said cross-bar switches connect CPUs and a memory within a computer, or perform switching between nodes of a multinode system having CPUs and memories wherein the memories of remote nodes are accessed via 5 the cross-bar switches.

11. The system according to claim 2, wherein said cross-bar switches connect CPUs and a memory within a computer, or perform switching between nodes of a multinode system having CPUs and memories wherein the memories of remote nodes are accessed via 5 the cross-bar switches.

12. The system according to claim 3, wherein said cross-bar switches connect CPUs and a memory within a computer, or perform switching between nodes of a multinode system having CPUs and memories wherein the memories of remote nodes are accessed via 5 the cross-bar switches.

13. The system according to claim 4, wherein said cross-bar switches connect CPUs and a memory within a computer, or perform

switching between nodes of a multinode system having CPUs and memories wherein the memories of remote nodes are accessed via  
5 the cross-bar switches.

14. The system according to claim 6, wherein said cross-bar switches connect CPUs and a memory within a computer, or perform switching between nodes of a multinode system having CPUs and memories wherein the memories of remote nodes are accessed via  
5 the cross-bar switches.

15. The system according to claim 1, wherein M and N are equal values.

16. The system according to claim 2, wherein M and N are equal values.

17. The system according to claim 3, wherein M and N are equal values